

Our Reference: 42P13835D

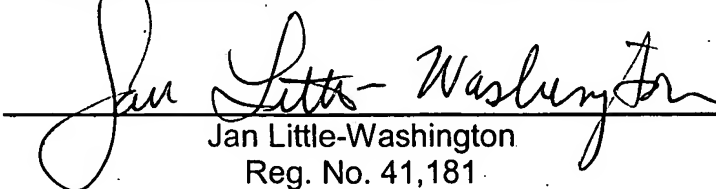
Patent

HIGH REFLECTOR TUNABLE STRESS COATING, SUCH AS FOR A MEMS MIRROR

Inventor: Michael Goldstein

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP


Jan Little-Washington
Reg. No. 41,181

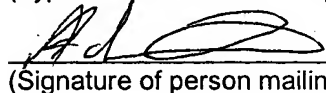
"Express Mail" mailing label number: EV320119360US

Date of Deposit: February 18, 2004

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Adrian Villarreal

(Typed or printed name of person mailing paper or fee)

 February 18, 2004
(Signature of person mailing paper or fee) (Date signed)

BEST AVAILABLE COPY

| | |
|---|---|
| Serial/Patent No. <u>New Patent Application</u> | Filing/Issue Date: <u>Herewith</u> |
| Client: <u>Intel Corporation</u> | |
| Title: <u>HIGH REFLECTOR TUNABLE STRESS COATING, SUCH AS FOR A MEMS MIRROR</u> | |
| BSTZ File No. <u>42P13835D</u> | Atty/Secty Initials: <u>JCL/av</u> |
| Date Mailed: <u>February 18, 2004</u> | Docket Due Date: _____ |
| The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon: | |
| <input type="checkbox"/> Amendment/Response (____ pgs.) | <input checked="" type="checkbox"/> Express Mail No.: <u>EV320119360US</u> <input checked="" type="checkbox"/> Check No.: <u>3367</u> |
| <input type="checkbox"/> Appeal Brief (____ pgs.) (in triplicate) | <input type="checkbox"/> _____ Month(s) Extension of Time Amt: <u>\$1050.00</u> |
| <input type="checkbox"/> Application - Utility (____ pgs. with cover and abstract) | <input checked="" type="checkbox"/> Information Disclosure Statement & PTO-1449 (<u>3</u> pgs.) <input type="checkbox"/> Check No. _____ |
| <input type="checkbox"/> Application - Rule 1.53(b) Continuation (____ pgs.) | <input type="checkbox"/> Issue Fee Transmittal Amt: _____ |
| <input checked="" type="checkbox"/> Application - Rule 1.53(b) Divisional (<u>19</u> pgs.) | <input type="checkbox"/> Notice of Appeal |
| <input type="checkbox"/> Application - Rule 1.53(b) CIP (____ pgs.) | <input type="checkbox"/> Petition for Extension of Time |
| <input type="checkbox"/> Application - Rule 1.53(d) CPA Transmittal (____ pgs.) | <input type="checkbox"/> Petition for _____ |
| <input type="checkbox"/> Application - Design (____ pgs.) | <input checked="" type="checkbox"/> Postcard |
| <input type="checkbox"/> Application - PCT (____ pgs.) | <input type="checkbox"/> Power of Attorney (____ pgs.) |
| <input type="checkbox"/> Application - Provisional (____ pgs.) | <input type="checkbox"/> Preliminary Amendment (____ pgs.) |
| <input type="checkbox"/> Assignment and Cover Sheet | <input type="checkbox"/> Reply Brief (____ pgs.) |
| <input checked="" type="checkbox"/> Certificate of Mailing | <input type="checkbox"/> Response to Notice of Missing Parts |
| <input checked="" type="checkbox"/> Declaration & POA (<u>5</u> pgs.) (copy) | <input type="checkbox"/> Small Entity Declaration for Indep. Inventor/Small Business |
| <input type="checkbox"/> Disclosure Docs & Orig & Copy of Inventor's Signed Letter (____ pgs.) | <input checked="" type="checkbox"/> Transmittal Letter, in duplicate |
| <input checked="" type="checkbox"/> Drawings: <u>3</u> # of sheets includes <u>7</u> figures | <input checked="" type="checkbox"/> Fee Transmittal, in duplicate |
| <input checked="" type="checkbox"/> Other: <u>Certificate of Mailing with copy of return postcard signed by the attorney; Copies of thirteen (13) cited references.</u> | |

APPLICATION FOR UNITED STATES LETTERS OF PATENT

FOR

**HIGH REFLECTOR TUNABLE STRESS COATING, SUCH AS FOR A MEMS
MIRROR**

Inventors: **Michael Goldstein**


Prepared by:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP
12400 Wilshire Boulevard, 7th Floor
Los Angeles, California 90025
(206) 292-8600

"Express Mail" Label Number EV320119360US

Date of Deposit February 18, 2004

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Mail Stop Patent Application, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

 February 18, 2004
Adrian Villarreal Date

**HIGH REFLECTOR TUNABLE STRESS COATING, SUCH AS FOR A
MEMS MIRROR**

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application is a Divisional of U.S. Application No. 10/079,614, filed February 19, 2002.

BACKGROUND OF THE INVENTION

10 1. Field of the Invention

 The present invention is related to optical networks and, in particular, to a coating for a micro-electromechanical systems (MEMS) mirror.

 2. Background Information

15 Integrated circuits are formed on semiconductor wafer substrates by a number of processing steps. These steps include deposition, etching, implantation, doping, and other semiconductor processing steps well known to those skilled in the art. Thin films can be formed on wafer surfaces by a deposition process as well. These thin films can comprise, for example, silicon dioxide, doped glasses,
20 silicides, etc. The thickness of such films usually ranges from about a few hundred angstroms to several micrometers. Often, three or more film layers are formed on the surface of a single semiconductor wafer. Deposition of such films can cause stress on the wafer, however.

25 In the art of fabricating semiconductor wafers, it is of known importance to minimize or control stresses in surface films. High surface stresses can cause the wafer to be deformed. For example, a compressive stress in a surface film will cause a wafer to slightly bow in a convex direction, while a tensile stress in a

surface film will cause a wafer to slightly bow in a concave direction. Therefore, both compressive and tensile stresses cause the surface of the semiconductor wafer to deviate from exact planarity.

5 Lowering the temperature used when depositing a film can reduce stresses. Unfortunately, lowering the deposition temperature tends to lower the quality of the devices that will use the wafer. For example, when wafer processing is used in the manufacture of a micro-electromechanical system (MEMS) mirror, the stresses may tend to cause the mirror to bow slightly, and these deviations in the mirror's shape
10 tend to cause coupling losses. MEMS mirrors tend to be very thin, on the order of a micron, and are particularly sensitive to stress. This is especially troublesome considering that current MEMS mirrors already tend to suffer from poor wavelength dependence, relatively low reflectivity, and other limitations, such as bandwidth and/or data rate limitations.

15

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally equivalent elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the reference
20 number, in which:

Figure 1 is a cross-section view of a photonic device according to an embodiment of the present invention;

25 Figure 2 is a perspective view of the high reflector coating of Figure 1 disposed on MEMS mirror, which is tuned to have compressive stress according to an embodiment of the present invention;

Figure 3 is a perspective view of the high reflector coating of Figure 1 disposed on MEMS mirror, which is tuned to have substantially no stress according to an embodiment of the present invention;

5 Figure 4 is a perspective view of the high reflector coating of Figure 1 disposed on MEMS mirror, which is tuned to have tensile stress according to an embodiment of the present invention;

10 Figure 5 is a graphical representation of a reflectance spectrum of the high reflector coating of Figure 1 in response to incident light near the 1260-1620 nm band in Figure 1 according to an embodiment of the present invention as related to metallic reflectors;

15 Figure 6 is a graphical representation of an angular spectrum of the high reflector coating of Figure 1 in response to incident light near 1550 nm in Figure 1 according to an embodiment of the present invention as related to metallic reflectors; and

20 Figure 7 is a flowchart of an approach to making a photonic device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

25 Embodiments of the present invention are directed to a multiple layer coating for a photonic device. The coating prescription provides a tunable stress that may be varied from tensile to compressive, a tunable index of refraction that may be varied from low to high, and a tunable shape for the resulting optical device that may be varied from concave to convex. Within the wavelength band of interest, the coating also exhibits high reflectivity (e.g., greater than approximately ninety-nine percent)

and wavelength independence. The photonic device may be a micro-electromechanical system (MEMS) mirror such as for a MEMS mirror-based optical cross-connect (OXC) switch or optical add/drop multiplexer (OADM). Such photonic-devices may be fabricated using standard semiconductor or MEMS
5 processes (e.g., standard deposition temperatures).

In the following description, numerous specific details, such as particular processes, materials, devices, and so forth, are presented to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will
10 recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, etc. In other instances, well-known structures or operations are not shown or described in detail to avoid obscuring embodiments of various embodiments of the invention.

15 Some parts of the description will be presented using terms such as stress, silicon, reflectivity, spectrum, reflectance, and so forth. These terms are commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art.

20 Various operations will be described as multiple discrete blocks performed in turn in a manner that is most helpful in understanding the invention. However, the order in which they are described should not be construed to imply that these operations are necessarily order dependent or that the operations be performed in the order in which the blocks are presented.

25

Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure, process, block, or characteristic described in connection with the embodiment is included in at least

one embodiment of the present invention. Thus, the appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be
5 combined in any suitable manner in one or more embodiments.

Figure 1 is a cross-section view of a photonic device 100 according to an embodiment of the present invention. The example photonic device 100 includes a multiple layer coating 101 and a base 102. The multiple layer coating 101 includes
10 a layer of silver (Ag) 104 on the base 102, a layer of silicon oxide (SiO_2) 106 on the layer of Ag 104, a layer of silicon (Si) 108 on the layer of SiO_2 106, and a layer of silicon oxynitride (SiO_xN_y) 110 on the layer of Si 108.

In an alternative embodiment of the present invention, the layer 104 may be
15 a layer of gold (Au) rather than Ag. Alternatively still, the silicon dioxide (SiO_2) layer 106 may include a different dielectric material, such as silver dioxide (AgO_2), for example, or may include a second layer of silicon dioxide (SiO_2) along with a layer of Ag O_2 .

20 Each layer 104, 106, 108, and 110 of the example photonic device 100 has certain physical properties. For example, the layer of Ag 104 has a physical thickness of at least approximately one hundred nanometers, the layer of SiO_2 106 has a physical thickness of approximately two hundred seventy nanometers, and the layer of Si 108 has a physical thickness of approximately fifty nanometers. The
25 layer SiO_xN_y 110 has a physical thickness that varies from approximately one hundred ten nanometers. The layer SiO_xN_y 110 also has a percentage of N_y that varies from approximately sixty percent N_y to twenty percent N_y .

Each layer 104, 106, 108, and 110 of the example photonic device 100 also has optical properties. For example, the layer of SiO_2 106 has an optical thickness of approximately one quarter of a wavelength of interest within a band of wavelengths of interest, the layer of Si 108 has an optical thickness of approximately 0.41 quarter of the wavelength, and the layer SiO_xN_y 110 has an optical thickness of approximately 0.44 quarter of the wavelength.

The photonic device 100 has a stress that may be tunable from tensile to compressive. For example, in embodiments in which the ratio of N_y is approximately sixty percent N_y , the photonic device stress is tensile. In embodiments in which the ratio of N_y is approximately forty percent N_y , the photonic device experiences no significant stress. In embodiments in which the ratio of N_y is approximately twenty percent N_y , the photonic device stress is compressive.

15

Of course, other ratios of N_y are possible and persons of ordinary skill in the relevant art(s) will readily recognize how to implement other stresses by varying the ratio of O_x to N_y in the layer SiO_xN_y 110. These methods include, but are not limited to, changes in contaminant levels (such as hydrogen), deposition rate, deposition temperature, buffer gas selection and pressures, as well as ion bombardment assisted deposition.

20

The photonic device 100 has an index of refraction that is tunable from low to high. For example, in embodiments in which the ratio N_y is approximately sixty percent N_y , the photonic device index of refraction is relatively high (e.g., approximately 2.0). In embodiments in which the ratio of N_y is approximately twenty percent N_y , the photonic device index of refraction is relatively low (e.g., approximately 1.44). Of course, other ratios of N_y are possible and persons of

25

ordinary skill in the relevant art(s) will readily recognize how to implement other indices of refraction by varying the ratio of N_y to other material components in the layer primarily made of SiO_xN_y 110.

5 The optical path length through the multiple layer coating 101 is held substantially constant by adjusting the layer SiO_xN_y 110 physical thickness in inverse proportion to the change in index of refraction. Of course, the exact stress values and indices of refraction may depend on photonic device 100 fabrication process conditions, such as temperature of deposition of the layers, rate of
10 deposition of the layers, ion bombardment deposition of the layers, and content of hydrogen and/or other impurities in plasma deposition. The fabrication process is described below with reference to Figure 7.

 The base 102 may be a substrate, such as a silicon, silicon-on-insulator
15 (SOI), glass, aluminum oxide, silicon-on-sapphire (SOS) substrate, or other suitable substrate. Alternatively, the base 102 may be a micro-electromechanical system (MEMS) mirror. Other suitable bases will be readily apparent to persons of ordinary skill in the relevant art(s).

20 The photonic device 100 has a shape that may vary from concave to convex. For example, in embodiments in which the ratio of N_y is approximately twenty percent N_y , the photonic device shape is convex. Figure 2 illustrates a convex photonic device 200 according to embodiments of the present invention.

25 In embodiments in which the ratio of N_y is approximately forty percent N_y , the photonic device shape is substantially flat. Figure 3 illustrates a flat photonic device 300 according to embodiments of the present invention.

In embodiments in which the ratio of N_y is approximately sixty percent N_y , the photonic device shape is concave. Figure 4 illustrates a concave photonic device 400 according to embodiments of the present invention. Of course, other ratios of N_y are possible and persons of ordinary skill in the relevant art(s) will readily recognize how to implement other shapes by varying the ratio of N_y in the layer SiO_xN_y 110.

The photonic device 100 exhibits high reflectivity (e.g., greater than approximately 99.5 percent) within a wavelength band of interest. Figure 5 is a graphical representation of a reflectance spectrum 500 of the multiple layer coating 101 in response to incident light near the 1260-1620 nm band according to an embodiment of the present invention as related to metallic reflectors. The reflectance spectrum 500 includes an "x" axis 502, which represents wavelength in nanometers, and a "y" axis 504, which represents reflectance in percentage.

The reflectance spectrum 500 includes a curve 506, which represents the reflectance (or reflectivity) of the multiple layer coating 101 for light having a wavelength in a range of approximately 1260 nm to 1620 nm. The reflectance spectrum 500 also compares the reflectance of the multiple layer coating 101 to the reflectance of silver (curve 508), gold (510), copper (512), and aluminum (514). This illustrates that the multiple layer coating 101 also exhibits substantial wavelength independence. Note that the reflectance of the multiple layer coating 101, silver, gold, and copper are substantially flat across the range of wavelengths. However, only the multiple layer coating 101 has a reflectance greater than ninety-nine percent over such a broad band of wavelengths.

Figure 6 is a graphical representation of an angular spectrum 600 of the multiple layer coating 101 in response to incident light near 1550 nm according to

an embodiment of the present invention as related to metallic reflectors. The reflectance spectrum 600 includes an "x" axis 602, which represents angle of incidence of light in degrees, and a "y" axis 604, which represents reflectance in percentage.

5

The angular spectrum 600 includes a curve 606, which represents the reflectance (or reflectivity) of the multiple layer coating 101 for light having a wavelength in a range of approximately 1550 nm (which is near the middle of standard communication windows, e.g., between C-band and L-band). The reflectance spectrum 600 also compares the reflectance of the multiple layer coating 101 to the reflectance of silver (curve 608), gold (610), copper (612), and aluminum (614). The angular spectrum 600 illustrates that the multiple layer coating 101 also exhibits substantial independence across a broad range of angles of incidence (e.g., approximately zero to sixty degrees). Note that only the multiple layer coating 101 has a reflectance greater than ninety-nine percent over such a broad range of angles of incidence.

That the photonic device(s) 100, 200, 300, 400, and other photonic device according implemented according to embodiments of the present invention exhibit high reflectivity in the second and third communication windows (e.g., ITU II, C-band, L-band, S-band) and minimal optical aberrations indicates that such photonic devices are not bandwidth or data rate limited. For example, such optical devices will be suitable for use as/in optical cross-connects (OXC) and/or optical add/drop multiplexers (OADM) that operate at the optical carrier level 192 (OC-192), which has a data rate of 9.95328 Gigabits per second (Gbps). Alternative embodiments of the present invention may be suitable for use as/in optical cross-connects (OXC) and/or optical add/drop multiplexers (OADM) that operate at OC-768, which has a data rate of 39.81312 Gbps.

Figure 7 is a flowchart of a process 700 for making a photonic device according to an embodiment of the present invention. A machine-readable medium having machine-readable instructions thereon may be used to cause a processor to perform the process 100. In general, the process 100 is implemented using standard semiconductor and MEMS fabrication techniques, such as implantation, doping, evaporation, chemical-vapor deposition, physical vapor deposition, ion assisted deposition, magnetron sputtering, electron beam sputtering, evaporation, masking, reactive ion etching, and/or other semiconductor processing techniques well known to those skilled in the art.

A block 702 forms a layer of silver (Ag) on a substrate. The layer of Ag may have a physical thickness of at least approximately one hundred nanometers.

A block 704 forms a layer of silicon dioxide (SiO_2) on the layer of Ag. The layer of silicon dioxide (SiO_2) may have a physical thickness of approximately two hundred seventy nanometers and an optical thickness of approximately one quarter of a wavelength for a wavelength of interest.

A block 706 forms a layer of silicon (Si) on the layer of SiO_2 . The layer of silicon (Si) may have a physical thickness of approximately fifty nanometers and an optical thickness of approximately forty-one one-hundredths of one quarter of the wavelength of interest in the material.

A block 708 forms a layer of silicon oxynitride (SiO_xN_y) on the layer of silicon (Si). The layer of SiO_xN_y may have a physical thickness within a range from of approximately one hundred nanometers to one hundred ten nanometers, a ratio of N_y within a range from approximately sixty percent N_y to twenty percent

N_y , and an optical thickness of approximately 0.44 quarter of the wavelength in the material.

Embodiments of the invention can be implemented using hardware,
5 software, or a combination of hardware and software. In implementations using software, the software may be stored on a computer program product (such as an optical disk, a magnetic disk, a floppy disk, etc.) or a program storage device (such as an optical disk drive, a magnetic disk drive, a floppy disk drive, etc.).

10 The above description of illustrated embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.
15 These modifications can be made to the invention in light of the above detailed description.

The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification and the
20 claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.